1. A method comprising:

forming a chalcogenide access device having a snapback voltage low enough to avoid disturbing data stored in a memory element while reading the memory element selected by the access device.

2. The method of claim 1 including forming the chalcogenide access device to have a snapback voltage less than the threshold voltage of the memory element.

3. The method of claim 2 including forming the memory element of a phase change material.

4. The method of claim 2 including forming the memory element of a thin film material.

5. The method of claim 1 including forming at least two arrays of memory elements stacked one on top of the other.

6. The method of claim 5 including forming memory arrays with at least two memory elements each having a chalcogenide access device.

7. The method of claim 6 including forming said chalcogenide access devices above a semiconductor substrate.

8. The method of claim 7 including forming said memory elements above said semiconductor substrate.

9. The method of claim 8 including forming an access device over a memory element.

10. The method of claim 9 including forming the access device directly on top of the memory element without an intervening barrier layer.

11. A memory comprising:

a cell including a chalcogenide access device and a memory element, the chalcogenide access device having a snapback voltage low enough to avoid disturbing data stored in the memory element while reading the memory element.

12. The memory of claim 11 wherein said chalcogenide access device has a snapback voltage less than the threshold voltage of the memory element.

13. The memory of claim 12 wherein said memory element includes a phase change material.

14. The memory of claim 12 wherein said memory element includes a thin film material.

15. The memory of claim 11 including at least two memory arrays, each array including a plurality of cells stacked one on top of the other.

16. The memory of claim 15 including at least two memory elements each having a chalcogenide access device.

17. The memory of claim 16 including a semiconductor substrate, said chalcogenide access devices of said two memory elements formed above said semiconductor substrate.

18. The memory of claim 17 wherein said two memory elements are formed above said semiconductor substrate.

19. The memory of claim 18 including an access device located over at least one of the two memory elements.

20. The memory of claim 19 wherein the access device is directly on top of the memory element.

21. A system comprising:

a processor-based device;

a wireless interface coupled to said processor-based device; and

a memory coupled to said device, said memory including a cell with a chalcogenide access device and a memory element, the chalcogenide access device having a snapback voltage low enough to avoid disturbing data stored in the memory element while reading the memory element.

22. The system of claim 21 wherein said chalcogenide access device has a snapback voltage less than the threshold voltage of the memory element.

23. The system of claim 22 wherein said memory element includes a phase change material.

24. The system of claim 21 wherein said memory includes at least two arrays each having rows and columns, one of said arrays stacked above the other of said arrays.

25. The system of claim 24 including two memory elements each having a chalcogenide access device.

26. The system of claim 25 including a substrate, said chalcogenide access devices formed above said substrate.

27. The system of claim 26 wherein said memory elements are formed above said semiconductor substrate.

28. The system of claim 27 including an access device located over the memory element.

29. The system of claim 28 wherein the access device is directly on top of the memory element.

30. The system of claim 21 wherein said access device and said memory element include chalcogenide material and the chalcogenide material used in the access device and the memory element are different chalcogenide materials.

31. The system of claim 21 wherein said wireless interface includes a dipole antenna.